Computational Methods for Steady-State CMOS Latchup Simulation

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ABSTRACT

Robust computational techniques are presented for steady-state characterization of CMOS latchup via numerical device simulation. Of specific interest are efficient means of accurately evaluating knees in *IV* characteristics, corresponding to latchup triggering and holding points. Making use of continuation procedures and special initial guess strategies, more than an order of magnitude improvement in computational efficiency is demonstrated over previous approaches.

Numerical device simulation is well established as an approach to modeling latchup in CMOS technology. Its use has stemmed from the ability to accurately and unambiguously determine critical latchup thresholds directly from fabrication information, without any parameter fitting. The only recognized disadvantage is the associated computational expense which can be minimized in part through the use of efficient discretization and non-linear solution strategies [1,2] or possibly by reducing the spatial dimensionality of the problem [3]. However, additional computational difficulties remain as the results of interest for steady-state latchup modeling are the values of knees or limit points where dI/dV is unbounded on the characteristic *IV* curves, known as the triggering and holding points (see fig. 1). It is the concern of this work to develop efficient methods from determining these points to arbitrary precision *without user intervention*. This type of analysis is also of use in device problems other than latchup, including power devices and avalanche snap-back effects.

Previous approaches to computing both the triggering and holding points used strictly voltage or current boundary conditions. Significant expense was then incurred in the non-linear iteration, due primarily to the rapidly changing slope of the characteristic *IV* curves. The approach taken in this work is to use continuation methods [4,5], which trace *IV* curves by pseudo-arc-length σ rather than strictly voltage or current increments so that extreme changes in both are limited. Additionally, by proper selection of σ, *IV* curves of any type can be traced in a minimum number of bias points. These procedures are implemented much like standard current boundary conditions [6] using an auxiliary equation such as

$$\dot{I}_0 (I - I_0) + \dot{V}_0 (V - V_0) - \sigma = 0$$

where I_0, V_0 are the initial current and voltage values and $\dot{I}_0, \dot{V}_0$ are unit tangent vectors which can be computed directly. The application of this condition assures that if either I or V changes rapidly, the boundary increments are weighted proportionally leading to optimal non-linear performance. Additionally, the tangent information is extremely valuable for latchup computations as (1) it indicates when the knee has been passed and (2) cubic interpolation can be used to produce extremely accurate initial guesses for the non-linear iteration. Experiments with practical device structures have produced trigger points automatically to an accuracy of .01% typically within 5-6 bias points and 20-30 non-linear iterations.

Generally continuation is applied by starting at a low current bias point, e.g. zero bias, and tracing the *IV* curve resolving any knees as they are encountered. To avoid tracing the entire *IV* curve if only holding point information is desired, it might be preferable to start the search from above the knee (see fig. 1). The process by which the high-current starting point is obtained then becomes a critical issue. In conjunction with standard voltage boundary conditions where this strategy is necessary, transient triggering pulses of various types have been used [3]. Unfortunately, the expense in resolving the transients is enormous, and further

the required pulse magnitude is unknown. In this work, a novel initial guess strategy is used which allows direct *steady-state* computation of the high-current point. For a comprehensive set of practical examples, it is found that the total number of non-linear iterations required to obtain the high-current *IV* point from zero-bias is generally less than 20 compared to 300-400 for a typical transient simulation.

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[4] H. B. Keller, in *Applications of Bifurcation Theory*, Academic Press, 1977.
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[6] M. R. Pinto, et. al., "PISCES-IIB", Stanford University, Sept. 1985.

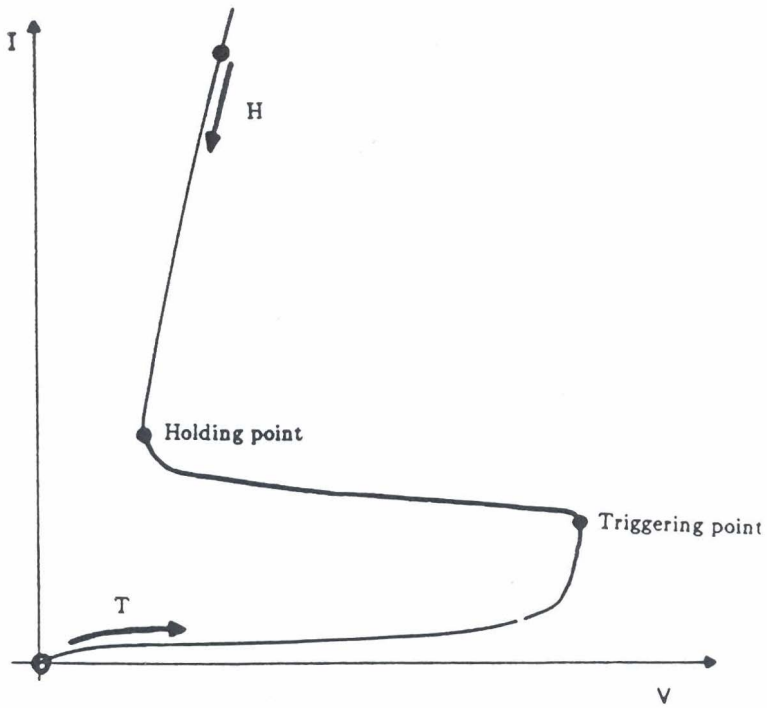

Figure 1 - Typical *IV* curve for steady-state latchup characterization in CMOS technology. The points of particular interest are the triggering and holding points, and the arrows labeled "T" and "H" denote the optimal *IV* search paths for each.